IN THE CLAIMS

Please amend the claims as follows:

1. (Previously presented) A circuit comprising:

a first edge-to-pulse converter having a first input to receive an initiating signal and a second input to receive a terminating signal, the first edge-to-pulse converter to provide an intermediate initiating signal at an output; and

a second edge-to-pulse converter having a first input to receive the intermediate initiating signal and a second input to receive the terminating signal, the second edge-to-pulse converter to provide a pulse having a width determined by a first edge of the intermediate initiating signal and a first edge of the terminating signal,

wherein each of the first and second converters performs an AND operation on the signals applied to its first and second inputs.

2. (Cancelled)

3. (Previously presented) The circuit of claim 1, wherein the AND operation is performed by first and second transistors coupled in series and having a first conductivity type, the gates of the first and second transistors forming the first and second inputs of the converters.

4. (Original) The circuit of claim 3, wherein each of the first and second converters further includes a pre-charge transistor coupled in series with the first and second transistors, a gate of the pre-charge transistor being coupled to the second input of its respective converter.

5. (Original) The circuit of claim 4, wherein the initiating and terminating signals are start and stop pulses, respectively, and the width of the intermediate initiating signal is determined by edges of the start and stop pulses.

6. (Original) The circuit of claim 1, wherein a trailing edge of the intermediate initiating signal is determined by a leading edge of the stop pulse.

7. (Original) The circuit of claim 1, wherein the first converter includes first, second and third transistors coupled in series between first and second reference voltages and an inverter coupled to a drain of the first transistor and the converter output.

8. (Original) The circuit of claim 7, wherein the first input is coupled to a gate of the second transistor and the second input is coupled to gates of the first and third transistors.

9 – 32 (Cancelled)